TITLE OF THE INVENTION

APPARATUS AND METHOD TO CORRECT A REFERENCE VOLTAGE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of Korean Application No. 2002-68486, filed November 6, 2002, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates to an apparatus and a method to correct a reference voltage, more especially to an apparatus and a method to correct a reference voltage to enable the reference voltage of electric devices to be corrected using software.

2. Description of the Related Art

[0003] Each of electric devices included in a digital system exchange data via a bus. The data exchanged via the bus has a digital form represented as an electrical 1 (high) or 0 (low). The electric devices recognize the data by recognizing a combination of 0 and 1 in transferred digital signals.

[0004] Accordingly, the electric devices have a reference voltage (Vref) to discriminate whether a received signal is 0 or 1. That is, if a voltage of the received signal is higher than the Vref, then the electric devices recognize the received signal as 1, or else if the voltage for the received signal is lower than the Vref, then the electrical devices recognize the received signal as 0.

[0005] FIG. 3 is a schematic view illustrating a circuit of a conventional device supplying the reference voltage Vref. Specifically FIG. 3 illustrates the circuit to supply the reference voltage Vref to two electric devices exchanging the digital data via the bus connected between each other.

[0006] As shown in FIG. 3, digital devices A and B 101 and 103 are provided to input/output the digital data between each other via a bus 105. The digital data is in a form of a signal electrically discriminated as 1 or 0, and, thus, the digital device A 101 and B 103 receive the Vref in order to discriminate the received signal.

[0007] The Vref is generally laid out so as to be output from a node between two resistors R1 120 and R2 106 connected in series to a VDD line, which is a main supply voltage of digital devices. The R1 120 and the R2 106 are fixed resistors and, thus, once laid out, it is impossible to adjust a resistance of the resistors R1 120 and R2 106.

[0008] Recently, as an operating speed of the electric devices is gradually increasing, noise in the digital data signal frequently occurs. Accordingly, accuracy of the Vref has been emphasized for accurate recognition of the digital data signal.

[0009] Also, in a case of transforming characteristics of the digital data signal with respect to (electromagnetic interference) EMI and, thus, tuning data transfer efficiency, the Vref is also to be adjusted according to the transformed data signal. In a case of adjusting the Vref, a user cannot manually connect resistors having different resistance values to a circuit in order to find appropriate new resistors R1 and R2 corresponding to an intended Vref, and if the user finds the appropriate new resistors R1 and R2, then the user has to change the old R1 and R2 to the new ones having an appropriate resistance value manually.

SUMMARY OF THE INVENTION

[0010] In accordance with an aspect of the present invention, there is provided an apparatus for reference voltage correction and a method therefor to enable a reference voltage of electric devices to be corrected using software.

[0011] Additional aspects and/or advantages of the invention will be set forth in part in the description which follows and, in part, will be obvious from the description, or may be learned by practice of the invention.

[0012] The foregoing and/or other aspects of the present invention are achieved by providing an apparatus for correcting a reference voltage (Vref) of a digital device to input/output digital data, including a Vref setup selecting part selecting a correction of the Vref; a Vref adjusting circuit adjusting the Vref of the digital device; and a Vref control storing part storing a Vref control program to change a setup of the Vref adjusting circuit to vary the Vref output from the Vref adjusting circuit to be varied, detecting a transmission state of the digital data of the digital device, determining an optimum setup of the Vref adjusting circuit to allow error bits of the digital data to be minimized, and setting up the Vref adjusting circuit according to selection of the Vref correction through the Vref setup selecting part.

[0013] According to an aspect of the present invention, the Vref control program includes a BIOS program.

[0014] According to an aspect of the present invention, the Vref adjusting circuit includes an adjustable resistor, and a fixed resistor to generate the Vref correction by dividing a main supply voltage of the digital device, wherein the Vref control program changes a resistance value of the adjustable resistor according to the selection of the Vref correction through the Vref setup selecting part, detects the transmission state of the digital data of the digital devices, determines an optimum resistance value of the adjustable resistor to allow the error bits of the digital data to be minimized, and sets up the resistance value of the adjustable resistor as the optimum resistance value.

[0015] According to an aspect of the present invention, the apparatus for correcting the reference voltage further includes a Vref optimum setup storing part to store data of optimum setup condition of the Vref adjusting circuit.

[0016] The foregoing and/or other aspects of the present invention are also achieved by providing a method to correct a reference voltage, Vref, of digital device having a Vref adjusting circuit to adjust the Vref, including selecting a reference voltage correction; changing a setup of the Vref adjusting circuit to vary the Vref; detecting a transmission state of digital data output from the digital device, according to the changed setup of the Vref adjusting circuit; determining an optimum setup of the Vref adjusting circuit to allow error bits of the digital data to be minimized; and setting up the Vref adjusting circuit according to the optimum setup.

[0017] According to an aspect of the present invention, there is provided a method to correct a reference voltage, Vref, between first and second digital devices using fixed and variable resistors, including: selecting a Vref correction via a BIOS setup menu; adjusting a resistance value of the adjustable resistor; loading a digital signal corresponding to a change of the resistance value of the adjustable resistor through a bus; confirming a state that the digital signal is transmitted; calculating an optimum resistance value of the adjustable resistor where a Vref correction is output to minimize error bits of the transferred digital signal; setting up the resistance value of the adjustable resistor as a calculated optimum resistance value; and storing the optimum resistance value.

[0018] According to an aspect of the present invention, there is provided an apparatus to correct a reference voltage, Vref, including: a first digital device and a second digital device inputting/outputting digital data via a bus; an adjustable resistor providing a main supply voltage

VDD; a fixed resistor, wherein the adjustable resistor and the fixed resistor generate a Vref correction by dividing the main supply voltage VDD; a Vref setup selecting part selecting the Vref correction; and a Vref controller changing a resistance value of the adjustable resistor according to a selection of the Vref correction through the Vref setup selecting part, determining an optimum resistance value of the adjustable resistor, and outputting an optimum Vref correction.

[0019] According to an aspect of the present invention, there is provided a method to correct a reference voltage, Vref, between first and second digital devices, including: selecting a Vref correction via a BIOS setup menu; adjusting a resistance value; loading a digital signal corresponding to a change of the resistance value through a bus; confirming a state that the digital signal is transmitted; calculating an optimum resistance value where a Vref correction is output to minimize error bits of the transferred digital signal; setting up the resistance value as a calculated optimum resistance value; and storing the optimum resistance value.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] These and/or other aspects and advantages of the present invention will become apparent and more readily appreciated from the following description of the embodiments, taken in conjunction with the accompany drawings of which:

FIG. 1 is a block diagram illustrating a control system of an apparatus to correct a reference voltage, according to an aspect of the present invention;
FIG. 2 is a flow chart illustrating a method to correct the reference voltage, according to an aspect of the present invention; and
FIG. 3 is a schematic view illustrating a circuit of a conventional device to supply the reference voltage.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0021] Reference will now be made in detail to the aspects of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to like elements throughout. The aspects are described below in order to explain the present invention by referring to the figures.

[0022] FIG. 1 is a block diagram illustrating a control system of an apparatus to correct a reference voltage, according to an aspect of the present invention. As shown in FIG. 1, the

apparatus for reference voltage correction includes a digital device A 1 and a digital device B 3 to input/output digital data via a bus 5, an adjustable resistor 18 and a fixed resistor 16 to generate a Vref (reference voltage) correction by dividing a main supply voltage VDD of the digital device A 1 and B 3, a Vref setup selecting part 10 to select the Vref correction, and a Vref controller 12 to change a resistance value of the adjustable resistor 18 according to a selection of the Vref correction through the Vref setup selecting part 10, thereby determining an optimum resistance value of the adjustable resistor 18 and outputting an optimum Vref. The Vref controller 12 allows setting up the adjustable resistor 18 so as to have the optimum resistance value. The apparatus also includes an optimum resistance storing part 14 to store the optimum resistance value.

[0023] The Vref setup selecting part 10 is provided for a user's selection of the Vref correction. Digital devices including the Vref correction may be of various types, such as a CPU, a memory, etc. Thus, the Vref setup selecting part 10 of a user interface adapted for one of the digital devices to be optimized, may be provided in a form of a BIOS menu.

[0024] The Vref controller 12 changes a resistance value of the adjustable resistor 18 by several mΩ, according to the selection of the Vref correction, and analyzes signals input into the digital device A 1 and the digital device B 3 by transmitting through the bus 5 a digital signal corresponding to the change of the resistance value of the adjustable resistor 18. The Vref controller 12 confirms a transmission state of the digital signal according to the change of the resistance value of the adjustable resistor 18 and, thus, confirms if error bits occur in the received signal. The Vref controller 12 calculates the optimum resistance value where the occurrence of the error bits is notably low and sets up the resistance value of the adjustable resistor 18 as the calculated optimum resistance value.

[0025] Furthermore, the Vref controller 12 stores the optimum resistance storing part 14 with the calculated optimum resistance value and sets up the resistance value of the adjustable resistor 18 as the optimum resistance value. Thus, until the optimum resistance value is set up again, the resistance value of the adjustable resistor 18 is set up as the calculated optimum resistance value, so that an optimum Vref can be provided.

[0026] The Vref controller 12 is implemented by software, such as a BIOS to perform the control process described above. Accordingly, the Vref setup selecting part 10 to select an optimum voltage setup of the digital devices A 1 and B 3 may be a BIOS setup menu provided by the BIOS.

[0027] As shown in FIG. 2, a Vref correction process for the apparatus using the reference voltage correction previously described is illustrated. Hereinafter, for illustrative purposes, it is assumed that the Vref controller 12 of the apparatus for the reference voltage correction is implemented using the BIOS software.

[0028] At operation S10, if the user selects a Vref correction via the BIOS setup menu, the Vref controller 12, or the BIOS adjusts the resistance value of the adjustable resistor 18. The Vref controller 12 transmits [loads a] the digital signal corresponding to the change of the resistance value of the adjustable resistor 18 through the bus 5, and, thus, at operation S14, confirms a state that the digital signal is transmitted. At operation S16, the Vref controller 12 calculates the optimum resistance value of the adjustable resistor 18 where the Vref correction is output to minimize the error bits of the transferred digital signal. At operation S18, the Vref controller 12 sets up the resistance value of the adjustable resistor 18 as the calculated optimum resistance value, and, at operation S20, stores the optimum resistance value. Accordingly, the digital device A 1 and B 3 can receive the optimum Vref. Further in a case that adjustment of the Vref is needed in the future, the Vref can be easily adjusted by repeating the above process.

[0029] In the meanwhile, in accordance with an aspect of the present invention, the resistance of the adjustable resistor is adjusted and set up, but according to an aspect of the present invention, the setup of the Vref adjusting circuit through which the optimum Vref is obtained may be maintained and updated by using software. Thus, an aspect of the present invention may be adapted to various kinds of circuits to adjust the Vref with the adjustable resistor.

[0030] With the above description, according to the present invention, when digital signals are transferred to a digital device, a Vref adjusting circuit determines, maintains, and updates an optimum Vref where error bits of the digital signals are minimized, to thereby enable the Vref to be corrected easily in an optimum condition.

[0031] As described above, according to the present invention, there is provided an apparatus and a method for correcting a reference voltage to enable the reference voltage to be corrected using software.

[0032] Although a few embodiments of the present invention have been shown and described, it will be appreciated by those skilled in the art that changes may be made in these

embodiments without departing from the principles and spirit of the invention, the scope of which is defined in the appended claims and their equivalents.